

Validation Using IPC Design Rules and Limitations to IPC-2221

In this chapter, the procedure developed earlier is applied to a simple three-dimensional model of a board and a trace, and the results are compared to experimental data reported in IPC 2221.

1. IPC-2221 Background

The ability of an etched or printed conductor to safely carry the electrical current necessary for a particular application (referred to as “current carrying capacity”) is an important property. In the majority of cases, the printed circuits are capable of carrying more electrical current than they ever encounter. However, there are a significant number of applications (some were discussed in chapter one), for which the designer must know with a reasonable degree of certainty whether a particular conductor can fulfill its requirements. To address this issue, in 1955, the National Bureau of Standards (NBS) was commissioned to establish a set of guidelines for sizing electrical traces on circuit boards. In 1956, the NBS team conducted a variety of experiments to provide

guidelines for determining the trace width as a function of trace thickness, the electrical current and the maximum permissible temperature rise. At the conclusion of the initial phase of this study, NBS researchers noticed a wide scatter of data points. They concluded that their results had many variables that required further investigation. Due to lack of funding, however, the effort was terminated prematurely, and the results were published as tentative guidelines for trace sizing (as shown in Figure 1).

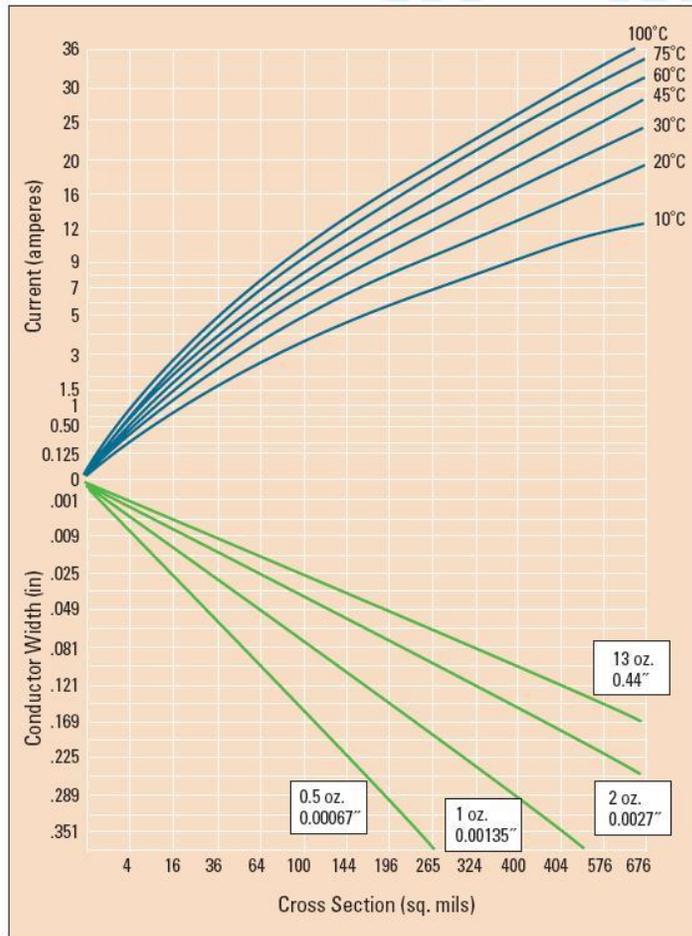
These graphs represent the upper limit of the data points [82]. The lower limit is in better agreement with the so-called “Design-News” correlations presented by Brooks [83].

Brooks suggests the following two fits for the two correlations, where I is in amps, ΔT is in °C, and A is in square mils for in both correlations:

$$I = 0.065 * \Delta T^{0.43} * A^{0.68} \quad \text{IPC Data} \quad (1)$$

$$I = 0.040 * \Delta T^{0.45} * A^{0.69} \quad \text{DN Data} \quad (2)$$

In reference [82] it is shown that these equations provide reasonable predictions for the Euro-format PCB (100mm x 160 mm x 1.6 mm) of bare epoxy with a single 1 oz (0.035 mm) copper trace. Equation (2) is used for PCB’s with no additional copper plane, while Equation (1) is suggested for use in applications with a 1-oz copper back plane. In both cases, it is assumed that the board and the trace are oriented vertically in the ambient air at 20 °C. In the next section a numerical model representing the above problem is presented.



2. Single Board with a Trace

Consider a printed circuit board, made of pure FR4, oriented vertically in quiescent ambient air at 20 C, as shown in Figure 2. The board is assumed to be 100 mm wide, 160 mm long and 1.6 mm thick and made of pure FR4. A single copper trace, 100 mm long, 8 mm wide and 0.035 mm thick (i.e., 1-oz copper), is etched on one side of the board. It is assumed that 10 amps of electrical current is flowing through the trace.

2.1 Cases Analyzed

Numerical simulations were performed for two cases. In Case 1 the model with geometry exactly as described above was simulated. In Case 2, a copper back plane (0.035 mm thick) was included in the model. The results of Case 1 are used for comparison with "Design News" data, whereas Case 2 results are used for comparison with "IPC" data.

2.2 Material Properties

The following material properties were used in the two models.

Board:	FR4	$k = 0.3 \frac{W}{m-K}$
--------	-----	-------------------------

Traces and Backplane:	Copper	$k = 395 \frac{W}{m-K}$
-----------------------	--------	-------------------------

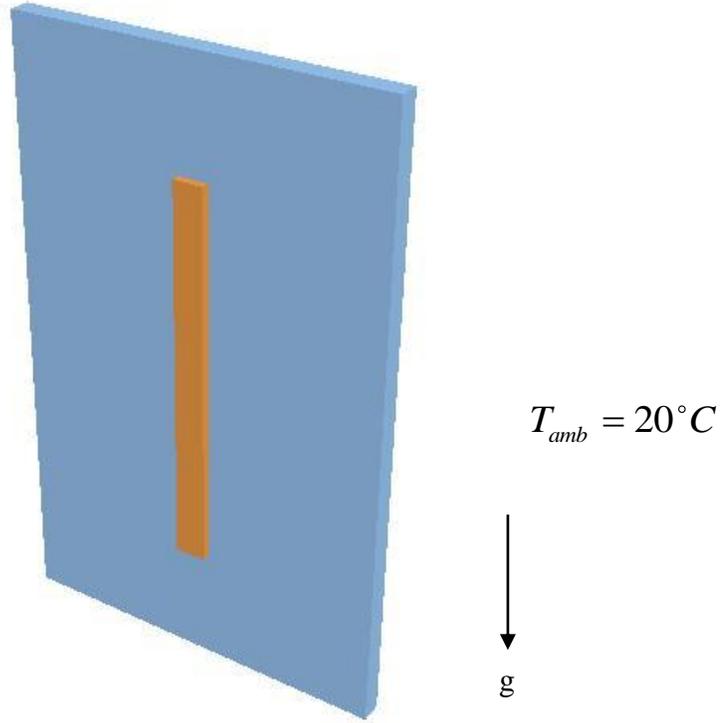


Figure 2: Vertical Board with a Single Trace

The electrical resistivity for copper is calculated from:

$$\rho_e = \rho_0 [1 + \alpha(T - T_0)]$$

$T_0 \equiv$ Reference Temperature = 20 °C

$\rho_0 \equiv$ Resistivity at T_0 = 0.0175e-06 $\Omega.m$

$\alpha \equiv$ Resistance Temperature Coefficients = 0.0039 °C⁻¹

2.3 *Model Details and Boundary Conditions*

The computational domain consisted of the board and an air region (extended by 24 mm on each side) surrounding the board. Approximately 48,000 non-uniform elements were used for discretization of this model. A much finer mesh was used near the solid surfaces as required by the steep gradients near the walls. Figure 3 illustrates the non-uniform mesh used for discretization of this problem

The only boundary conditions required for this model were two *Current BC's* to specify 10 amps of electrical current passing through the trace. It should be noted that no boundary conditions are necessary to specify air inflow and outflow regions. The program recognizes the “open” boundaries at the edges of the computational domain and applies inflow and outflow boundaries as needed based on the local pressure gradient.

Figures 4 and 5 illustrate the temperature and velocity fields for Case 1 and Case 2 respectively.

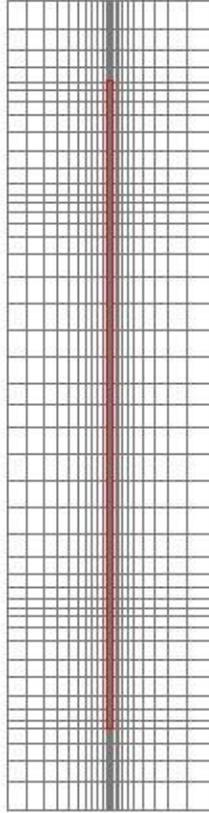
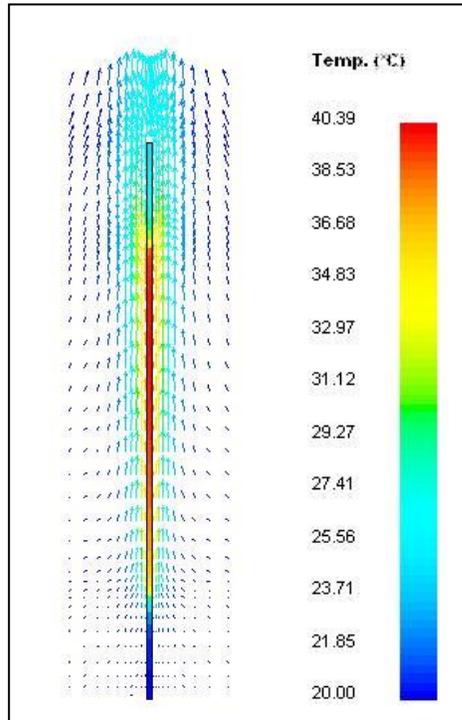
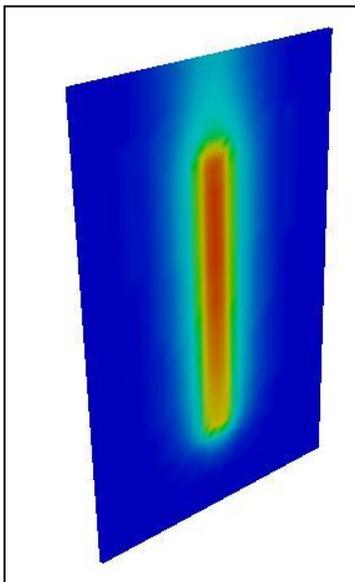


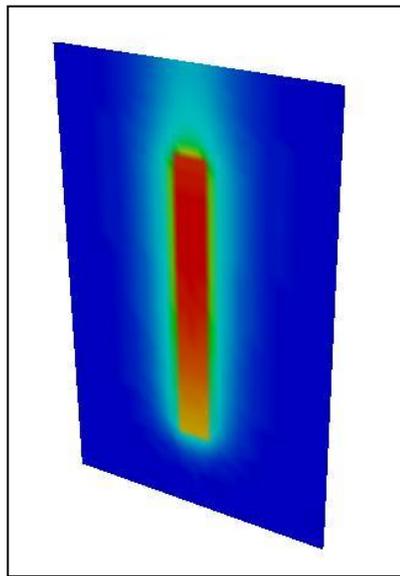
Figure 3: Mesh Used for Vertical Board with a Single Trace



a) Side View

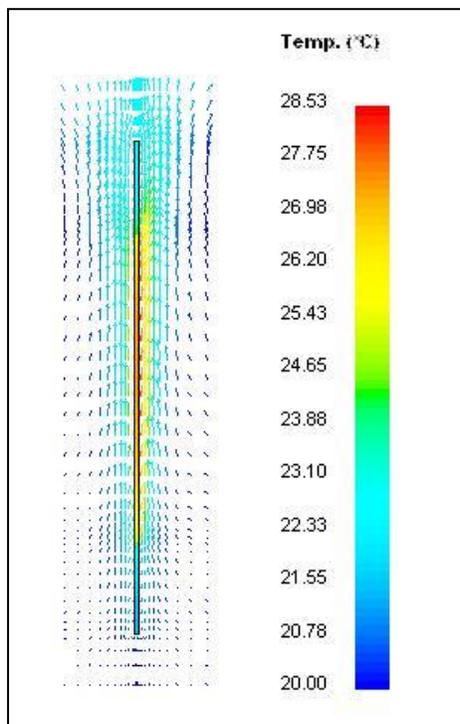


b) 3D View – Back of Board

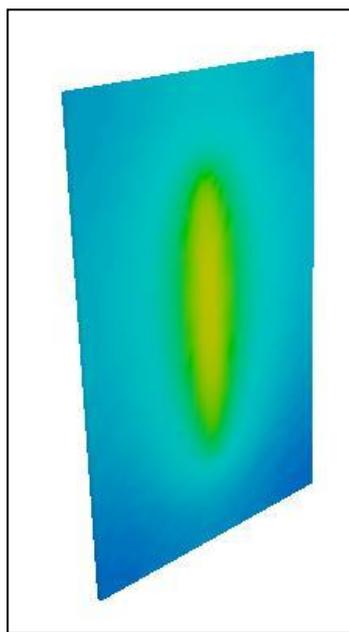


c) 3D View – Front of Board

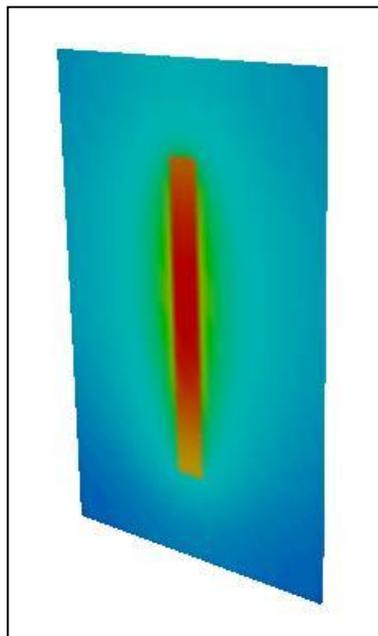
Figure 4: Temperature and Velocity Field – Vertical Board w/ No Back Plane



a) Side View



b) 3D View – Back of Board



c) 3D View – Front of Board

Figure 5: Temperature and Velocity Field – Vertical Board - with Back Plane

2.4 Comparison with Test Data

Equation (2) and (1) can be used to obtain the predicted average temperature rise using DN and IPC test data (corresponding to Case 1 and Case 2 numerical models).

DN Comparison:

$$I = 0.040 * \Delta T^{0.45} * A^{0.69} \text{ with } I=10 \text{ amps, and } A=434 \text{ mil}^2$$

$$\Rightarrow \Delta T_{DN} = 19.257^\circ C$$

$$\% \Delta = \frac{|\Delta T_{DN} - \Delta T_{Sim}|}{\Delta T_{DN}} \times 100 = \frac{|19.257 - 19.244|}{19.257} \times 100 = 0.0675\%$$

IPC Comparison:

$$I = 0.065 * \Delta T^{0.43} * A^{0.68} \text{ with } I=10 \text{ amps, and } A=434 \text{ mil}^2$$

$$\Rightarrow \Delta T_{IPC} = 8.23^\circ C$$

$$\% \Delta = \frac{|\Delta T_{IPC} - \Delta T_{Sim}|}{\Delta T_{IPC}} \times 100 = \frac{|8.23 - 8.04|}{8.23} \times 100 = 2.308\%$$

Figure 6 shows these results in the form of a bar chart. As it is evident from these results, there is excellent agreement between numerical and experimental results.

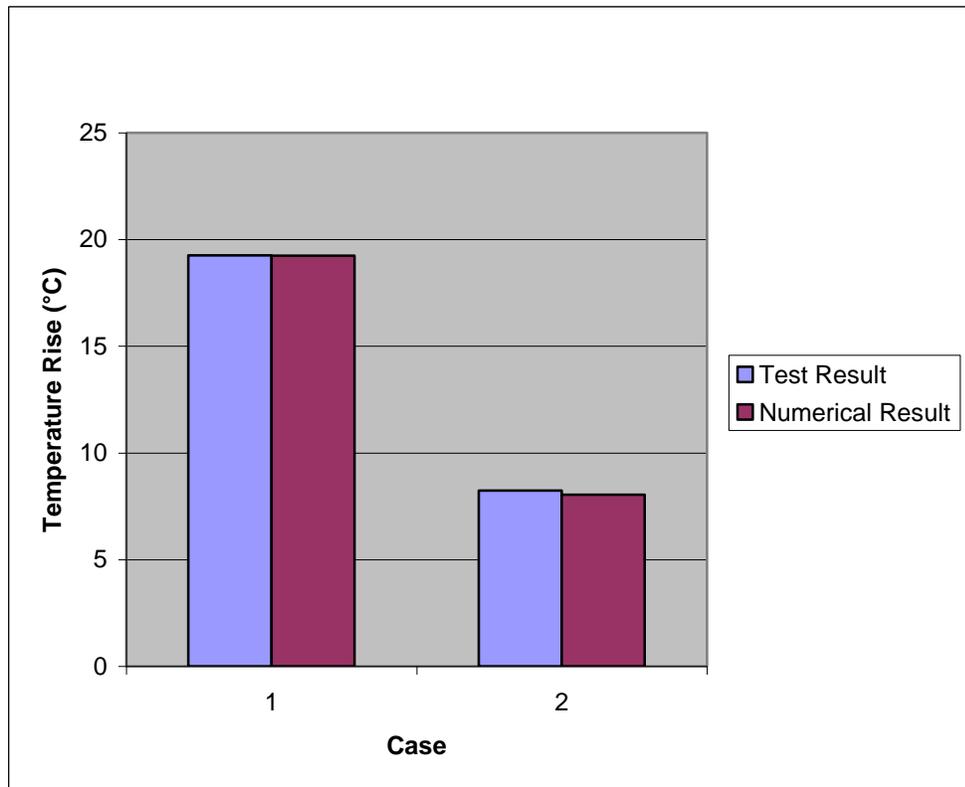


Figure 6: Comparison between Numerical and Experimental Results

3. Problems with IPC Design Rules

As previously mentioned, traditionally, trace sizing has been performed using the IPC charts which are based on tentative results relating electrical current, cross-sectional area and temperature rise. Soon after these results were published, they were adapted by the military and were included in MIL-STD-275. Over the years, the electronic packaging industry has turned to these charts for guidance, not paying close attention to what the information in the chart actually means. This lack of understanding of what the charts represent and how to work with them has generated significant confusion, leading to many flawed thermal designs.

Some of the factors to consider are presented in the following paragraphs:

- The tests were performed using only external traces, since back in 1955 there were no multi-layer boards with internal traces. There are, however, charts in use today that are used for internal traces. These charts were generated using the original charts for external traces but assuming half of the current, a very questionable assumption, indeed.
- The tests were performed using single and double sided phenolic and epoxy boards of varying thickness – some boards had a full copper plane on the backside, and some did not. Originally, the idea was to gain a better understanding of factors affecting the temperature rise in traces. But, since the research was stopped prematurely due to lack of funding, the NBS researchers

compiled all these results to produce the IPC charts. This implies that the charts represent an average with respect to variable in the test samples.

- The user of the chart must keep in mind that the predictions are for a specific board configuration with a single copper trace, suspended in air. A great majority of today's designs fall outside these conditions.

In the next section, we will examine the effect of enclosing the board on the trace temperature, and in the following section we will look at the effect of additional boards.

4. Single Board inside Enclosure

In the earlier examples, we considered cases involving a board with a single trace with no flow restrictions. In the next two sections, we will investigate the effect of placing the board inside an enclosure, and also, possible effects of other boards in close proximity on the trace temperature rise. The goal here is to check the accuracy of IPC predictions for realistic cases, and to determine whether they can be extrapolated beyond test conditions.

The board studied earlier is modeled inside an enclosure in a natural convection environment at 20 °C. The enclosure is 0.168 m long, 0.108 m wide and 0.07 m high and made out of plastic with thermal conductivity of 0.5 (W/m-K). The board is assumed to exist inside the enclosure (1.22 cm from the bottom wall) with no contacts between the enclosure walls and the board and a 2 mm gap between the enclosure walls and the edges of the board. Figure 7 shows the enclosure with the board.

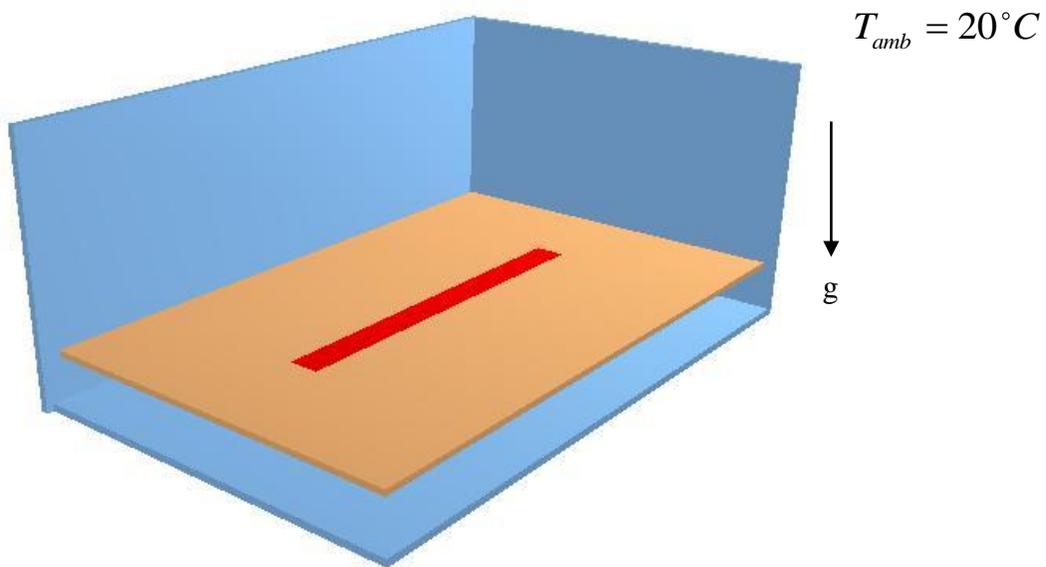


Figure 7: Enclosure and Board Geometry

4.1 Model Details

For this model, the computational domain was extended to the edges of the enclosure.

Approximately 43,000 non-uniform elements were used for discretization of this model (Figure 8).

4.1 Boundary Conditions

As before, the *Current BC's* were used to specify 10 amps of electrical current passing through the trace. Also, since the computational domain is terminated at the edges of the enclosure, convection heat transfer boundary conditions are used to account for the transfer of the heat from the enclosure to the ambient. The standard correlations for natural convective heat transfer from vertical and horizontal surfaces are used in this model. These correlations are presented in Appendix C.

4.2 Analysis

The numerical simulations for the steady-state solution were performed using Eflo software, using *Full-CFD* options with electrical and radiation solvers enabled.

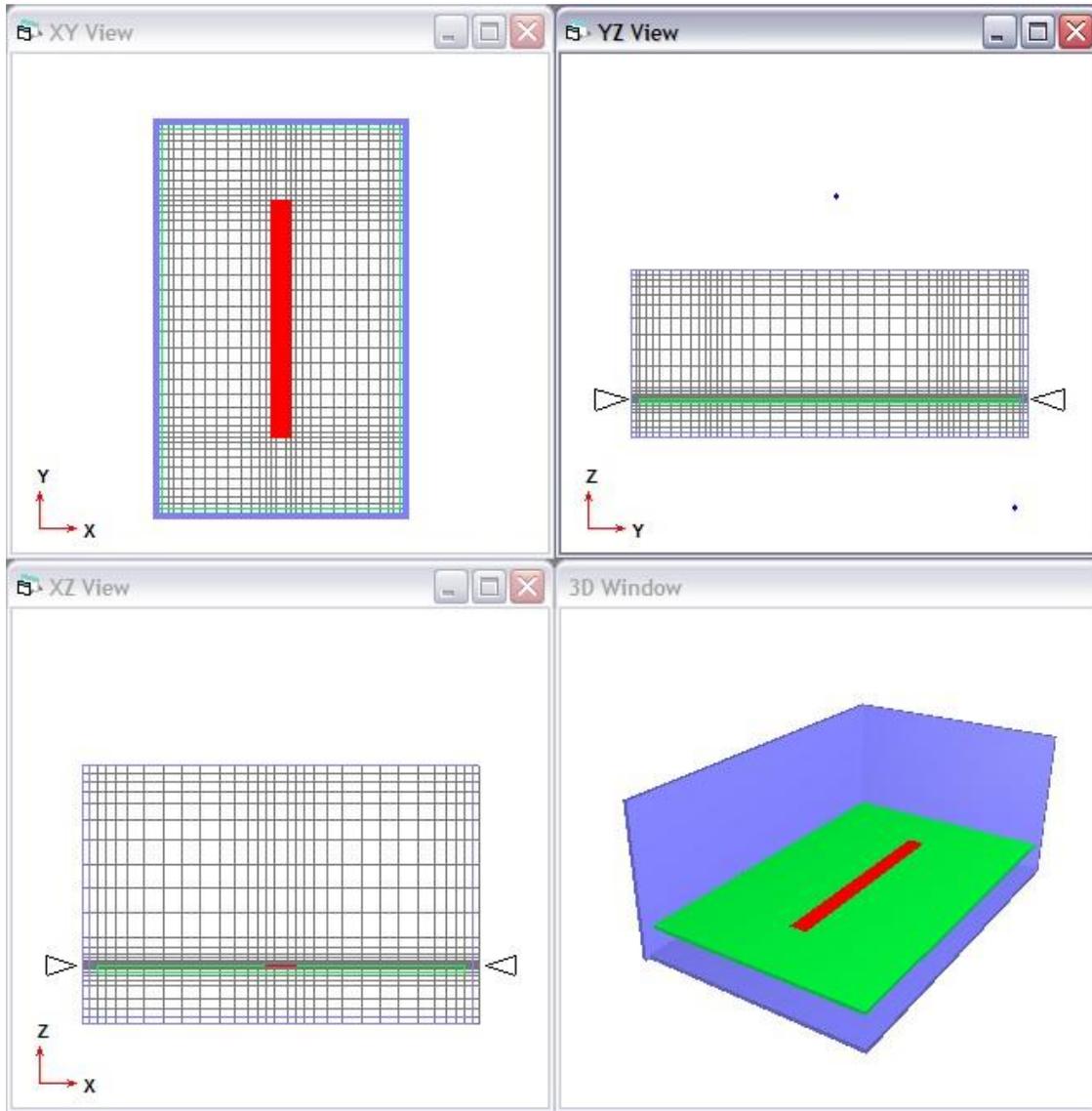


Figure 8: Finite Volume Mesh

4.3 Results

The numerical analysis predicts a maximum velocity of 9.75 cm/sec and a maximum trace temperature of 49.9 °C. This corresponds to a temperature rise of 29.9 °C, which is 10 degrees (roughly 50 %) higher than predicted by IPC results.

Figure 9 shows the two- and three-dimensional temperature fringe plots. The temperature distribution on a plane passing through the board is presented in Figure 9 (a). Figure 9 (b) and (c) show the combined temperature and velocity distribution. Note that velocity vectors are colored according to the nodal temperature and sized according to the velocity magnitude. Figure 9 (b) depicts a surface plot of temperature/velocity on a “yz” plane passing through the middle of the board and halving the trace lengthwise. Figure 9 (c) illustrates a similar result on an “xz” plane. These figures clearly show the resulting symmetric natural convective cells.

5. Multiple Boards inside Enclosure

To study the effect of a neighboring board on the trace temperature, the printed circuit board in the previous model was copied with 8.4 mm spacing between the two boards, as shown in Figure 10. All other parameters remain unchanged.

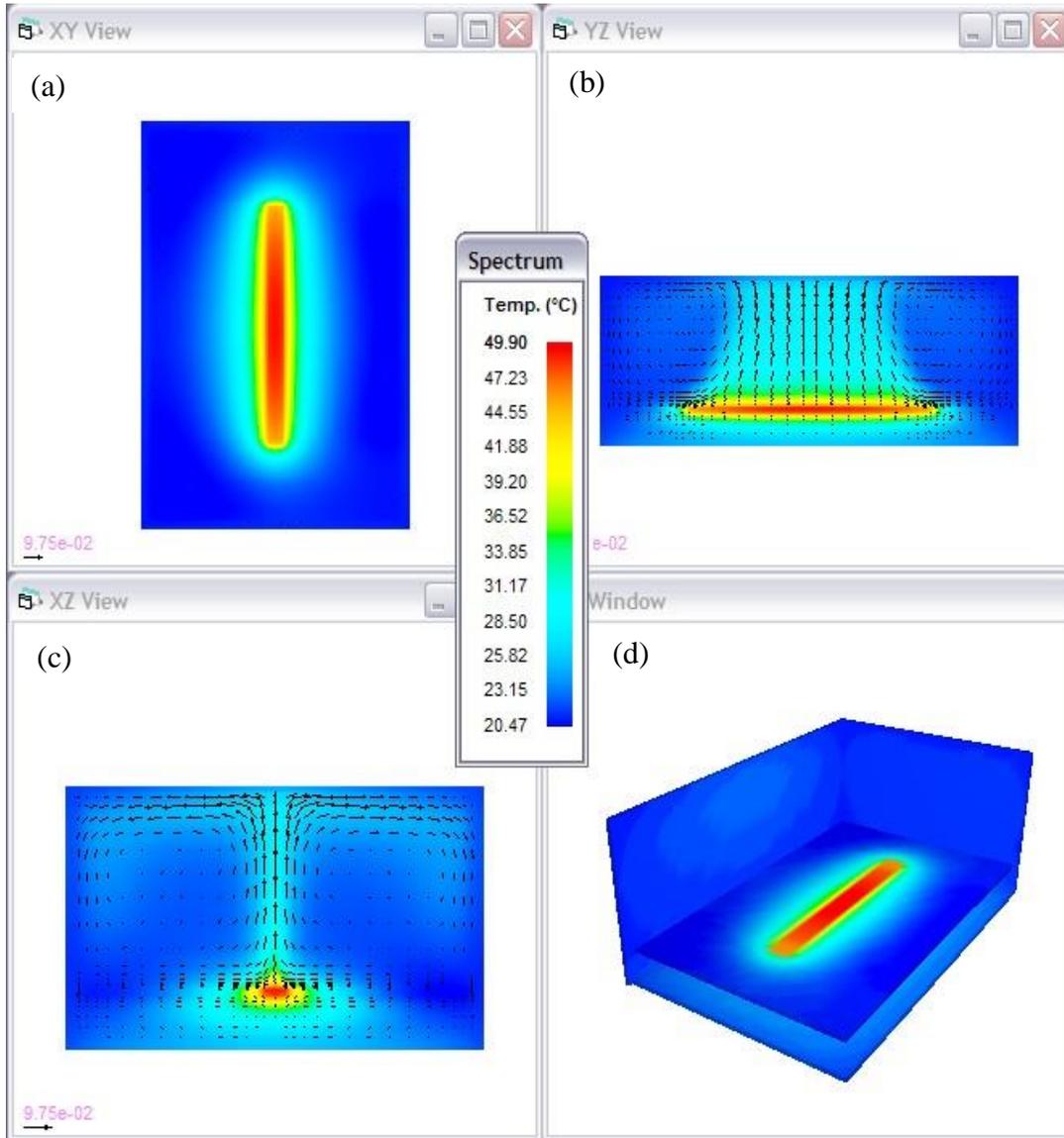


Figure 9 : Simulation Results

$$T_{amb} = 20^{\circ}C$$

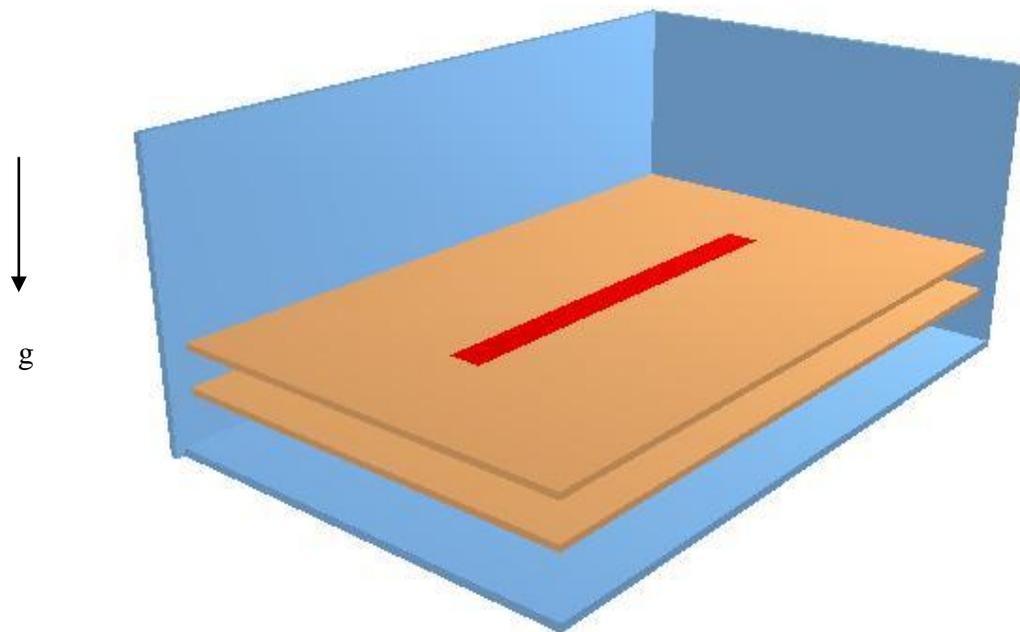


Figure 10: Enclosure with Two Boards

5.1 Analysis

A numerical model of the enclosure and the two boards were created using 57800 elements. The non-uniform mesh is illustrated in Figure 11. Boundary conditions used in this model are identical to those used in the model presented in section 5. However, with 10 amps of electrical current flowing through the traces on each board, the total Joulian heat dissipation inside the enclosure is roughly doubled.

The steady-state solution to this problem is obtained using coupled CFD, Thermal and Electrical procedure with surface-to-surface thermal radiation.

5.2 Results

The results of the numerical analysis are presented in Figure 12. These results indicate that, with the additional board in the enclosure, the maximum trace temperature has increased to 68.11 °C. This corresponds to an increase of 18.2 °C compared to one board in the enclosure and 27.7 °C compared to IPC results. The maximum velocity was found to be 12.6 cm/sec.

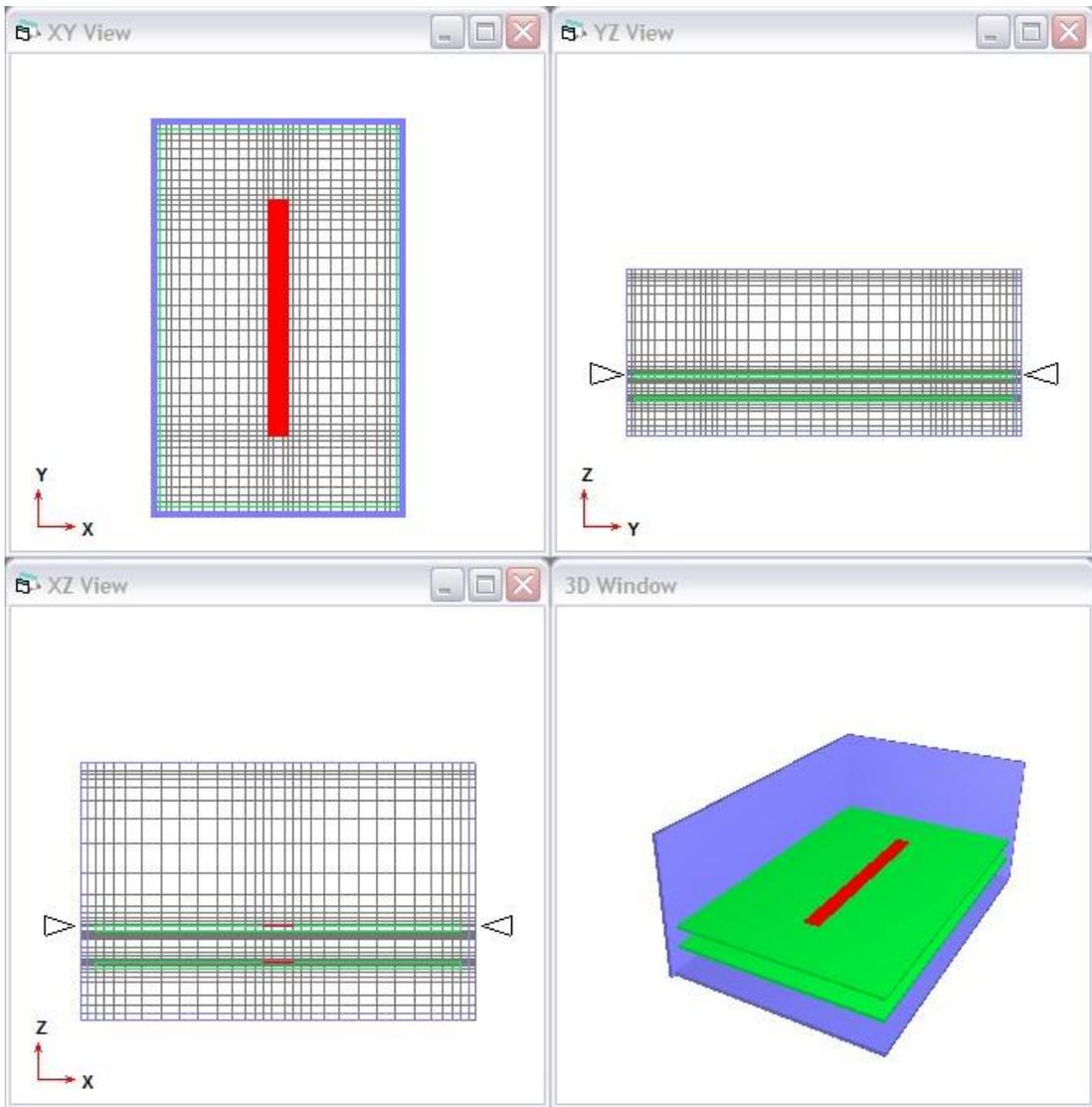


Figure 11: Finite Volume Mesh – Two Boards in Enclosure

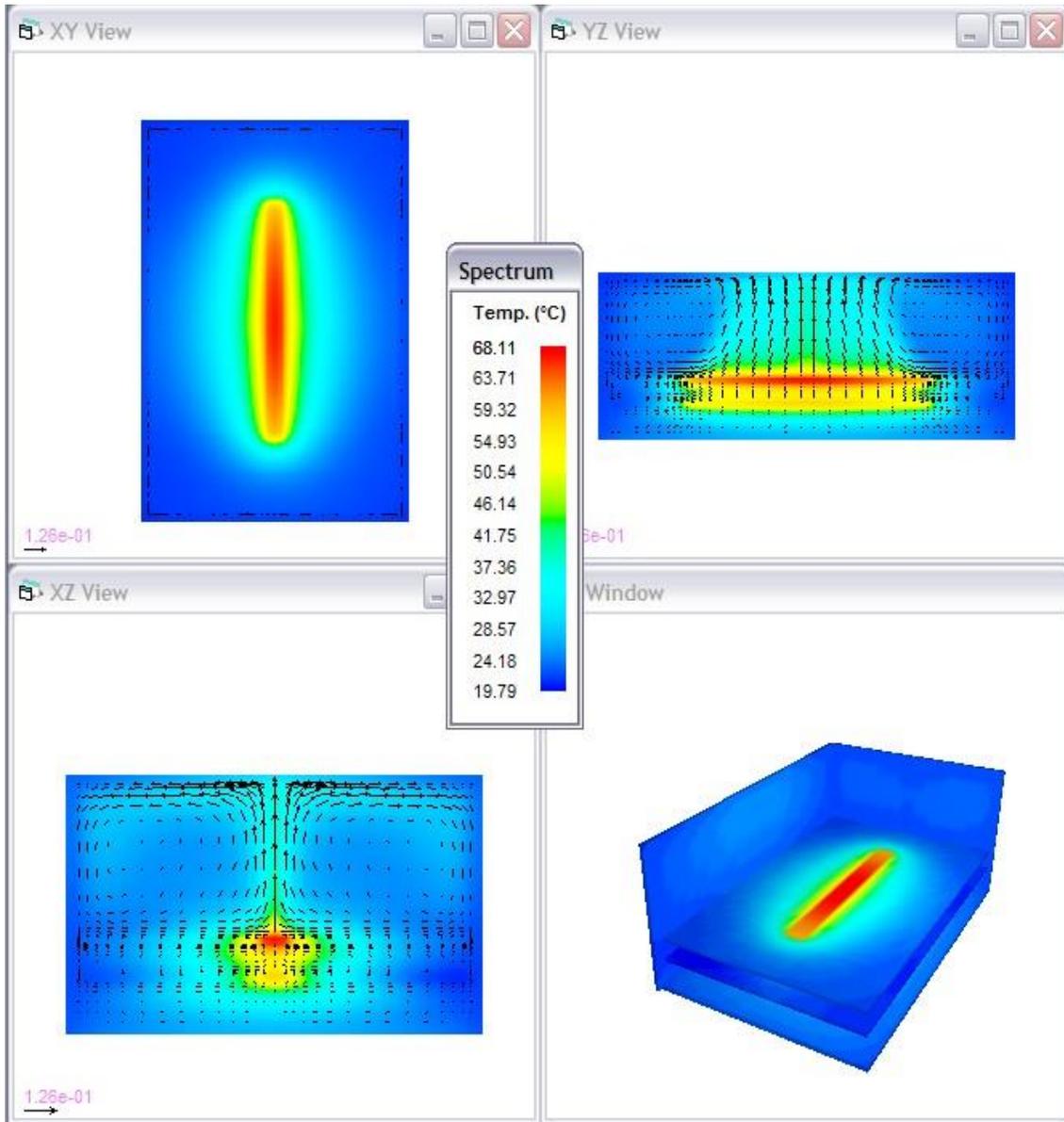


Figure 12: Simulation Results – Two Boards in Enclosure

6. Closing Remarks

Numerical results are shown to be in excellent agreement with both IPC and DN test results. The error in the DN case is 0.0675% and in the IPC case is 2.3%. Additional analyses, however, underscore the fact that while these test data predict the temperature rise for a single trace on a board remarkably well, they can be very misleading in more complex real world cases. For years, electronics design and packaging have been using the results of these tests to determine the current carrying capacity of traces. The thinking has been that a certain amount of current flowing through a given trace (with specified length and cross-sectional area) would result in a certain temperature rise in the trace. This, in fact, is not a correct statement. A much better statement would be that a certain amount of current flowing through a given trace would result in a certain amount of heat dissipation in that trace. The temperature rise in the trace, however, is determined by how efficiently this heat is transferred to the ambient. Some of the factors that can greatly affect the efficient transfer of heat are:

- Flow restrictions due to enclosure and adjacent boards
- Internal copper layers
- Other traces and components on the board.

This clearly shows that, in general, the prediction of a trace temperature rise requires a thorough heat transfer analysis. In other words, IPC based calculators represent oversimplification of complex problems. In fact, the designers are likely to get a far better estimate of the trace temperature from an educated guess.