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REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
-	RELEASED ON ECN #1079	10/26/00	MA
A	RELEASED ON ECN #1848	02/11/05	RM

1. **Specification subject to change without notice.**
2. **All dimensions are in millimeters.**
3. **Precautions: These precautions apply equally to modules from all makers, not just Densitron. Violation of these guidelines may void the warranty and can cause problems ranging from erratic operation to catastrophic display failure.**

Handling precautions:

- ◆ This device is susceptible to Electro-Static Discharge (ESD) damage. Observe Anti-Static precautions.

Power supply precautions:

- ◆ Identify and, at all times, observe absolute maximum ratings for both logic and LC drivers. Note that there is some variance between models.
- ◆ Prevent the application of reverse polarity to VDD and VSS, however briefly.
- ◆ Use a clean power source free from transients. Power up conditions are occasionally "jolting" and may exceed the maximum ratings of the module.
- ◆ The +5V power of the module should also supply the power to all devices which may access the display. Don't allow the data bus to be driven when the logic supply to the module is turned off.
- ◆ DO NOT install a capacitor between the Vo (contrast) pin and ground. VDD must, at all times, exceed the Vo voltage level. The capacitor combines with the contrast potentiometer to form an R-C network which "holds-up" Vo, at power-down, possibly damaging the module.

Operating precautions:

- ◆ DO NOT plug or unplug the module when the system is powered up.
- ◆ Minimize the cable length between the module and host MPU. (Recommended max. length 30 cm).
- ◆ For models with EL or CCFL backlights, do not disable the backlight by interrupting the HV line. Unloaded inverters produce voltage extremes which may arc within a cable or at the display.
- ◆ Operate the module within the limits of the modules temperature specifications.

Mechanical / Environmental precautions:

- ◆ Improper soldering is the major cause of module difficulty. Use of flux cleaner is not recommended as they may seep under the elastomeric connection and cause display failure. Densitron recommends the use of Kester "245" no-clean solder.
- ◆ Mount the module so that it is free from torque and mechanical stress.
- ◆ Surface of LCD panel should not be touched or scratched. The display front surface is an easily scratched, plastic polarizer. Avoid contact and clean only when necessary with soft, absorbent cotton dampened with petroleum benzene.
- ◆ ALWAYS employ anti-static procedure while handling the module.
- ◆ Prevent moisture build-up upon the module and observe the environmental constraints for storage temperature and humidity.
- ◆ DO NOT store in direct sunlight.
- ◆ If leakage of the liquid crystal material should occur, avoid contact with this material, particularly ingestion. If the body or clothing becomes contaminated by the liquid crystal material, wash thoroughly with water and soap.

Notes: (unless otherwise specified)

Unless otherwise specified: Dimensions are mm Tolerances are: X = ± 3 .X = ± 0.5 .XX = ± 0.05 CAGE CODE #OWS52	APPROVALS	DATE	<h1>DENSITRON CORPORATION</h1>	
	DRAWN			
	CHECKED		TITLE	LCD MODULE CUSTOM 640 X 200 GRAPHICS
	ISSUED		DWG. NO.	HC6642EUF0327

1.0 DESCRIPTION

Dot matrix display module consisting of liquid Crystal Display, LSI, printed circuit board, metal support frame and cold cathode fluorescent (CCFL) backlight

Available LC fluid types are: NTN (supertwisted nematic).

2.0 MECHANICAL CHARACTERISTICS

Item	Specifications	Unit
Package Dimensions	260.0 (W) x 110.7.0 (H) x 15.4 max (D)	mm
Display format	640 dots (W) x 200 dots (H)	-
Driving method	1/200	duty
Dot size	0.30 (W) x 0.366 (H)	mm
Dot pitch	0.33 (W) x 0.369 (H)	mm
Active display area	211.17 (W) x 79.17 (H)	mm
Viewing area	216.0 (W) x 83.2 (H)	mm

Notes: W-Width; H-Height; D-Depth.

3.0 LABELLING & MARKING

DENSITRONHC 6642EUF0327 TAIWAN YYMM

4.0 ABSOLUTE MAXIMUM RATINGS

VSS=0V; Ta=25°C

Item	Symbol	NTN		Unit
		Min.	Max.	
Logic supply voltage	VDD-VSS	0	7	V
LC driver supply voltage	VDD-VO	0	25	V
Operating temperature	TOP	-10	+50	°C
Storage temperature (Note 1)	TST	-20	+60	
Humidity: Operating (@40°C)	-	-	85%	RH (Note 2)
Non-operating (@40°C)	-	-	95%	RH (Note 2)

- Notes: 1: Tested to 100 hrs.
 2: Refers to non-condensing conditions.
 3. It is not recommended to operate CCF lamp below 0°C.

5.0 ELECTRICAL CHARACTERISTICS

VDD=5±0.25V; Ta=25°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input "High" voltage	V _{IH}	-	0.8	-	V _{DD}	V
Input "Low" voltage	V _{IL}	-	V _{SS}	-	0.2V _{DD}	V
Output "High" voltage	V _{OH}	I _{OH} =0.205mA	2.2	-	-	V
Output "Low" voltage	V _{OL}	I _{OL} =1.2mA	-	-	0.8	V
Power supply current	I _{EE}	V _{EE} =-20V	-	2.5	-	mA
Power supply current	I _{DD}	V _{DD} =5.0V	-	27	-	mA

6.0 RECOMMENDED LC DRIVE VOLTAGE (V_{DD}-V_O)

V_{DD}=5.0±0.25V

Temperature	NTN
T _a = -20°C	-
T _a = 0°C	22.8
T _a = 25°C	21.7
T _a = 50°C	20.8
T _a = 70°C	-

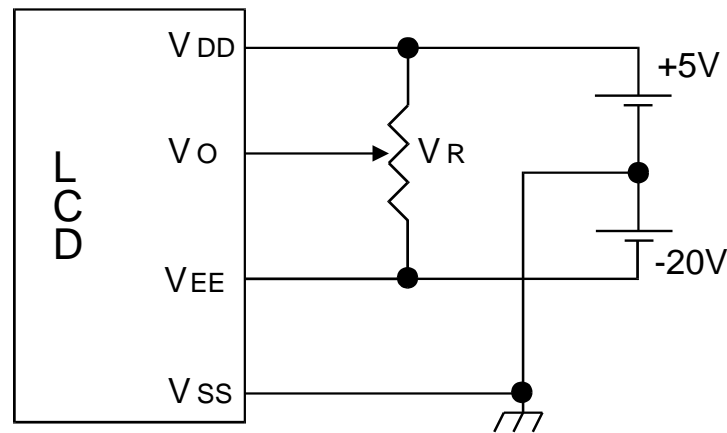
7.0 BACKLIGHT SPECIFICATIONS:

T_a=20°C,60%RH,Darkroom.

Item	Symbol	Typ.	Max.	Unit
CFL lamp input voltage	V _{CCFL}	250	300	V _{rms}
CFL input current	I _{CCFL}	5.0	6.0	mA
Life to half initial brightness	-	10000	15000	Hours
CFL lamp input frequency	F _{CCFL}	25	60	KHz
*Recommended backlight inverter	-	INV-12	-	-

*Note: Reference Application B on INV-12 specification

8.0 POWER SUPPLY

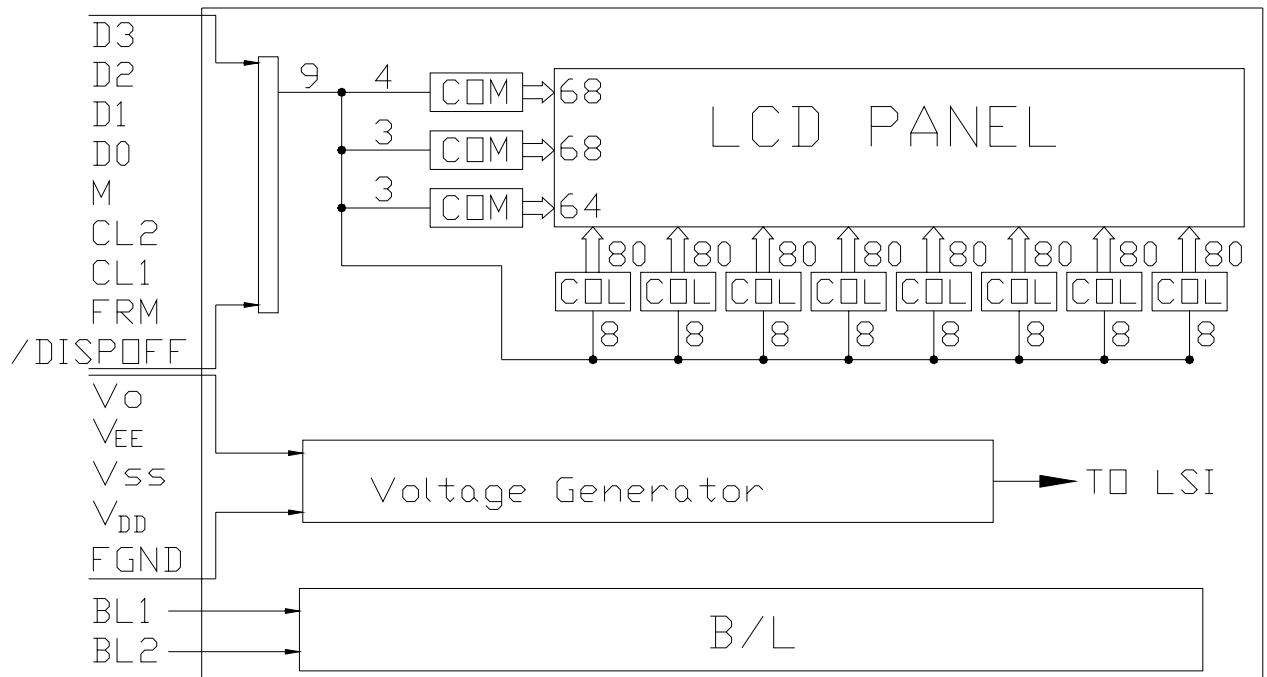


V_R = 10K - 20K ohm

9.0 INTERFACE DESCRIPTION

Pin No.	Symbol	I/O	Function
1	VDD	-	Power supply for logic circuit
2	FGND	-	Frame Ground
3	CL2	I	Clock signal for shifting the serial data
4	DISPOFF	I	"L": Display OFF "H": Display ON
5	FRM	I	First line marker indicates the beginning of each display cycle
6	CL1	I	The CL1 latches the serial data in the shift registers
7	Vss	-	Ground
8	M	I	Control signal for A.C. driving
9	D0	I	Bi directional data bus line 0
10	D1	I	Bi directional data bus line 1
11	D2	I	Bi directional data bus line 2
12	D3	I	Bi directional data bus line 3
13	VEE	-	Power supply for LC drive
14	Vo	-	Operating voltage for LCD drivers
15	Vss	-	Ground

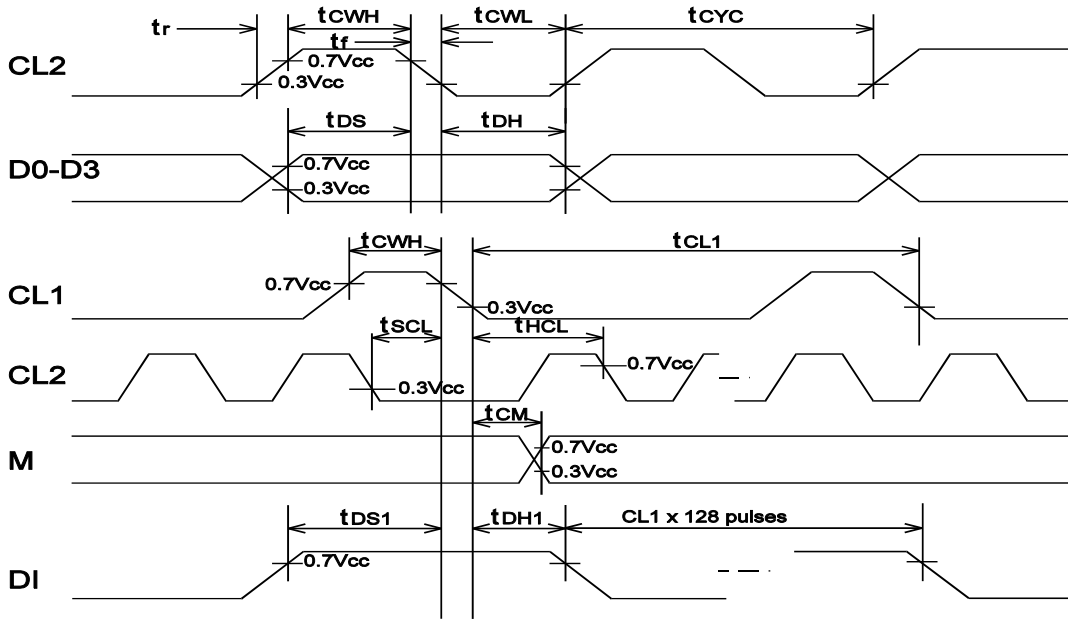
10.0 BLOCK DIAGRAM:



11.0 TIMING CHARACTERISTICS

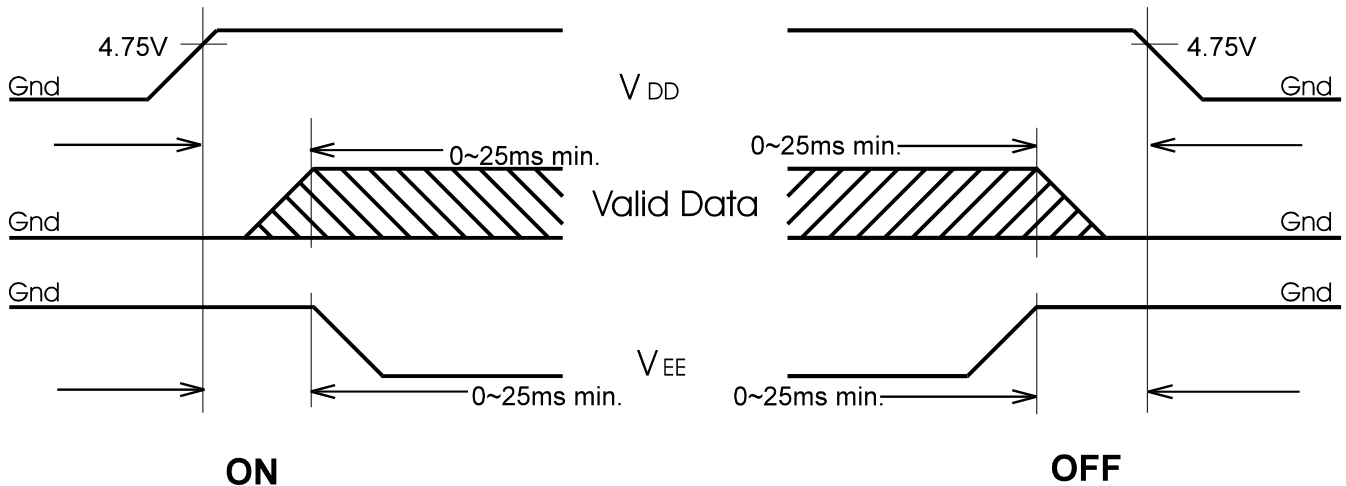
Item	Symbol	Min.	Typ.	Max.	Unit
Clock cycle time	t _{CYC}	200	-	-	nS
Clock high/low-level width	t _{CWH} , t _{CWL}	45	-	-	nS
Clock setup/hold time	t _{SCL} , t _{HCL}	80	-	-	nS
Clock rise/fall time	t _r , t _f	-	-	Note 1	nS
Data setup/hold time	t _{DS} , t _{DH}	20	-	-	nS
Setup/Hold time	t _{DS1} , t _{DH1}	100	-	-	nS
CL1 cycle time	t _{CL1}	t _{CYC} x 60	-	-	nS
M phase difference time	t _{CM}	-	-	300	ns

Note 1: $t_r, t_f < (t_{CYC} - t_{CWH} - t_{CWL})/2$ and $t_r, t_f \leq 30ns$



12.0 VOLTAGE SEQUENCING

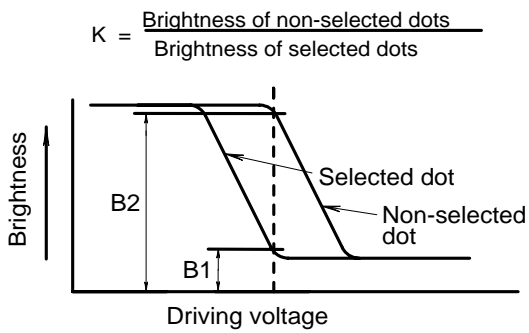
Always observe the following power supply ON/OFF sequence. Failure to so may cause latch up of CMOS LSI circuits or DC induced damage to LC panel.



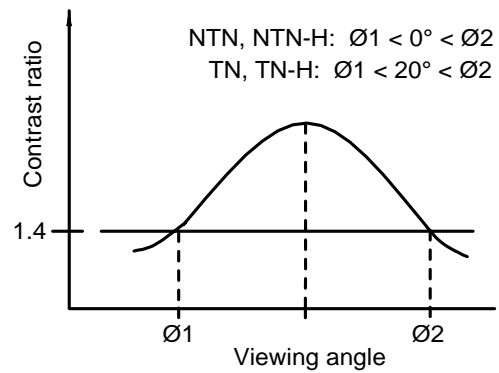
13.0 OPTICAL CHARACTERISTICS

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Contrast ratio	K	$\varnothing=20^\circ \theta=0^\circ$	3	-	-	-
Viewing angle	$\varnothing2-\varnothing1$	$\theta=0^\circ K \geq 1.4$	40	-	-	Deg.
	θ	$\varnothing=20^\circ K=1.4$	± 30	-	-	Deg.
Response time	Rise	$\varnothing=10^\circ \theta=0^\circ$	-	60	250	mS
	Fall	$\varnothing=10^\circ \theta=0^\circ$	-	130	450	mS

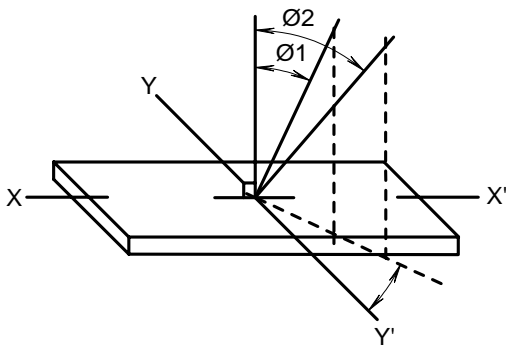
DEFINITION OF CONTRAST RATIO (K)



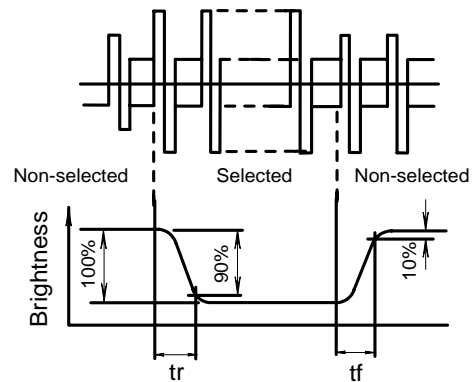
CONTRAST VERSUS VIEWING ANGLE

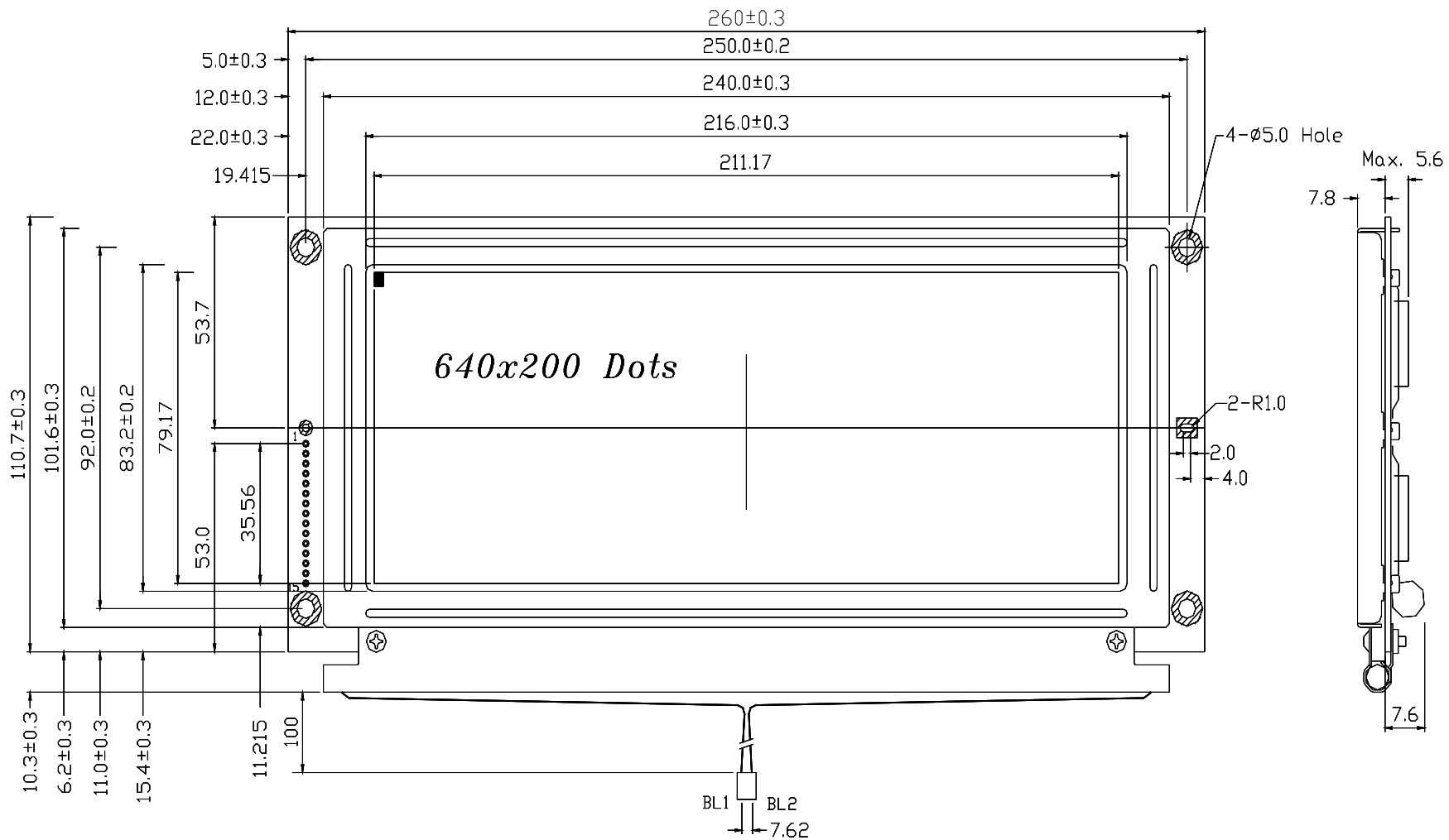


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DEFINITION OF OPTICAL RESPONSE





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