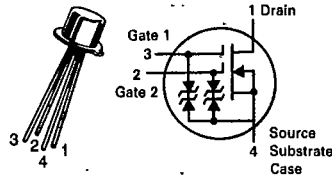


# MFE120 thru MFE122

CASE 20-03, STYLE 9  
TO-72 (TO-206AF)



**DUAL-GATE MOSFET  
VHF AMPLIFIERS**

**N-CHANNEL — DEPLETION**

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	+25	Vdc
Drain Current	$I_D$	30	mA <sub>dc</sub>
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 1.7	mW mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage ( $I_D = 100 \mu\text{A}_{dc}, V_S = 0, V_{G1S} = -4.0 \text{ V}, V_{G2S} = +4.0 \text{ V}$ )	$V_{(BR)DSX}$	25	—	—	Vdc
Gate 1-Source Breakdown Voltage ( $I_{G1} = \pm 10 \mu\text{A}_{dc}, V_{G2S} = 0$ )	$V_{(BR)G1SO}$	$\pm 7.0$	—	$\pm 20$	Vdc
Gate 2-Source Breakdown Voltage ( $I_{G2} = \pm 10 \mu\text{A}_{dc}, V_{G1S} = 0$ )	$V_{(BR)G2SO}$	$\pm 7.0$	—	$\pm 20$	Vdc
Gate 1 Leakage Current ( $V_{G1S} = +6.0 \text{ Vdc}, V_{G2S} = 0, V_{DS} = 0$ )	$I_{G1SS}$	—	—	20	nA <sub>dc</sub>
Gate 2 Leakage Current ( $V_{G2S} = +6.0 \text{ Vdc}, V_{G1S} = 0, V_{DS} = 0$ )	$I_{G2SS}$	—	—	20	nA <sub>dc</sub>
Gate 1 to Source Cutoff Voltage ( $V_{DS} = 15 \text{ Vdc}, V_{G2S} = 4.0 \text{ Vdc}, I_D = 200 \mu\text{A}_{dc}$ )	$V_{G1S(off)}$	—	—	-4.0	Vdc
Gate 2 to Source Cutoff Voltage ( $V_{DS} = 15 \text{ Vdc}, V_{G1S} = 0, I_D = 200 \mu\text{A}_{dc}$ )	$V_{G2S(off)}$	—	—	-4.0	Vdc

**ON CHARACTERISTICS**

Zero-Gate-Voltage Drain Current ( $V_{DS} = 15 \text{ Vdc}, V_{G1S} = 0, V_{G2S} = 4.0 \text{ Vdc}$ )		$I_{DSS}$	Min	Typ	Max	Unit
	MFE120		2.0	7.0	18	mA <sub>dc</sub>
	MFE121		5.0	10	30	
	MFE122		2.0	9.0	20	

**SMALL-SIGNAL CHARACTERISTICS**

Forward Transfer Admittance (Gate 1 to Drain) ( $V_{DS} = 15 \text{ Vdc}, V_{G2S} = 4.0 \text{ Vdc}, I_D = 10 \text{ mA}_{dc}, f = 1.0 \text{ kHz}$ )		$ Y_{fs} $	Min	Typ	Max	Unit
	MFE120,22 MFE121		8000 10,000	—	18,000 20,000	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = 15 \text{ Vdc}, V_{G2S} = 4.0 \text{ Vdc}, I_D = I_{DSS}, f = 1.0 \text{ MHz}$ )	MFE120,22 MFE121	$C_{iss}$	—	4.5 4.5	7.0 6.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 15 \text{ Vdc}, V_{G2S} = 4.0 \text{ Vdc}, I_D = 6.0 \text{ mA}_{dc}, f = 1.0 \text{ MHz}$ )		$C_{rss}$	—	0.023	—	pF
Output Capacitance ( $V_{DS} = 15 \text{ Vdc}, V_{G2S} = 4.0 \text{ Vdc}, I_D = I_{DSS}, f = 1.0 \text{ MHz}$ )	MFE120,22 MFE121	$C_{oss}$	—	2.5 2.5	4.0 3.5	pF

ELECTRICAL CHARACTERISTICS (continued) (T<sub>A</sub> = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>FUNCTIONAL CHARACTERISTICS</b>					
<b>Noise Figure</b> (V <sub>DS</sub> = 15 Vdc, V <sub>G2S</sub> = 4.0 Vdc, I <sub>D</sub> = 6.0 mA, Z <sub>S</sub> is optimized for NF) (f = 105 MHz — Figure 1) (f = 60 MHz — Figure 3) (f = 200 MHz — Figure 3)	MFE120 MFE121 MFE121	—	2.9	5.0	dB
<b>Common Source Power Gain</b> (V <sub>DS</sub> = 15 Vdc, V <sub>G2S</sub> = 4.0 Vdc, I <sub>D</sub> = 6.0 mA, Z <sub>S</sub> is optimized for NF) (f = 105 MHz — Figure 1) (f = 60 MHz — Figure 3) (f = 200 MHz — Figure 3)	MFE120 MFE121 MFE121	17	19.6	—	dB
<b>Level of Unwanted Signal for 1.0% Cross Modulation</b> (V <sub>DS</sub> = 15 Vdc, V <sub>G2S</sub> = 4.0 Vdc, I <sub>D</sub> = 6.0 mA)	—	—	100	—	mV
<b>Common-Source Conversion Power Gain (Gate 1 Injection, Figure 2)</b> (V <sub>DS</sub> = 15 Vdc, V <sub>G2S</sub> = 4.0 Vdc, Local Oscillator Voltage = 925 mVrms) (Signal Frequency = 60 MHz, Local Oscillator Frequency = 104 MHz) (Signal Frequency = 200 MHz, Local Oscillator Frequency = 244 MHz)	MFE122 MFE122	15	16.5	—	dB

FIGURE 1 — 60, 105 AND 200 MHz POWER GAIN AND NOISE FIGURE TEST CIRCUIT

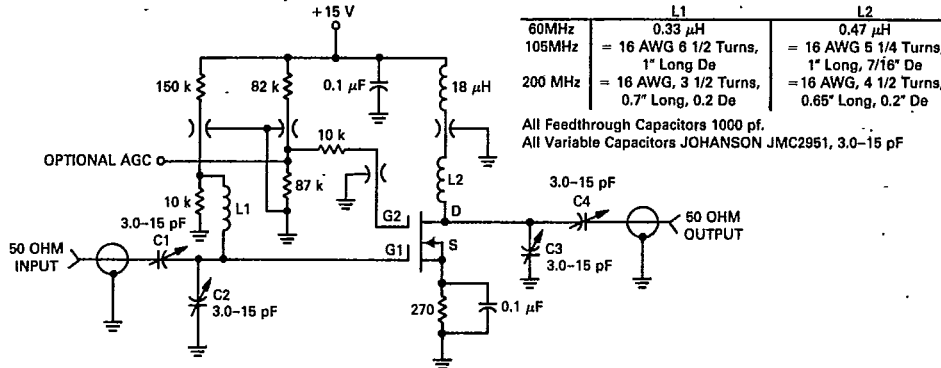
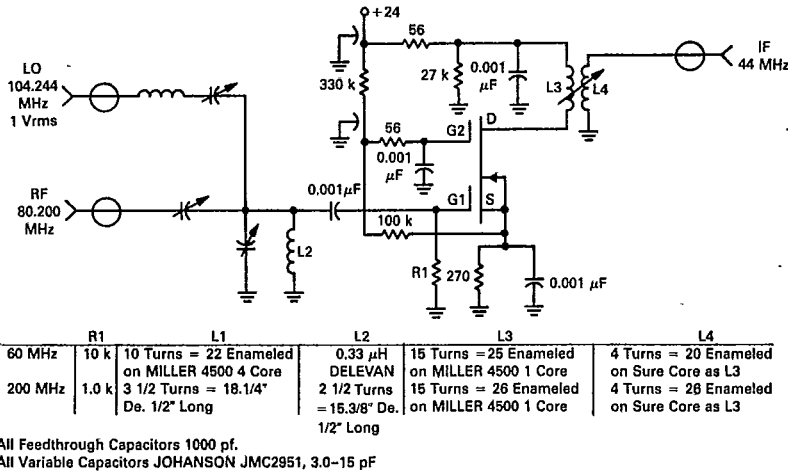


FIGURE 2 — 60 AND 200 MHz CONVERSION GAIN TEST CIRCUIT

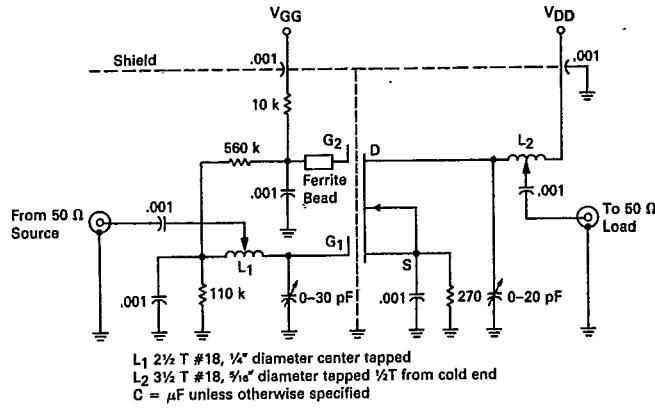


MOTOROLA SMALL-SIGNAL TRANSISTORS, FETs AND DIODES

MFE120 thru MFE122

T-31-25

FIGURE 3 - 60 AND 200 MHz CONVERSION POWER GAIN



COMMON-SOURCE ADMITTANCE PARAMETERS  
 ( $V_{DS} = 15$  Vdc,  $V_{G2S} = 4.0$  Vdc,  $I_D = 6.0$  mAdc)

FIGURE 4 - INPUT ADMITTANCE

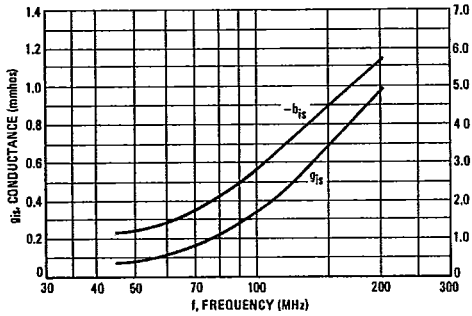


FIGURE 5 - REVERSE TRANSFER ADMITTANCE

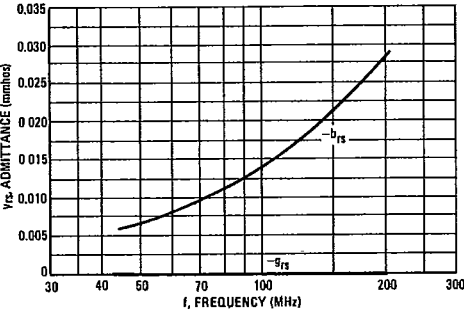


FIGURE 6 - FORWARD TRANSFER ADMITTANCE

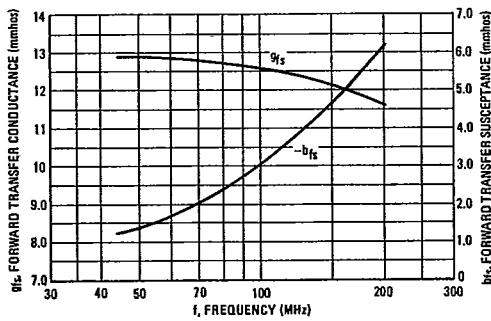
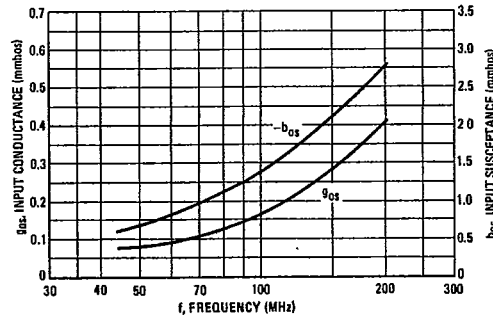


FIGURE 7 - OUTPUT ADMITTANCE



MFE120 thru MFE122

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FIGURE 8 - GAIN REDUCTION

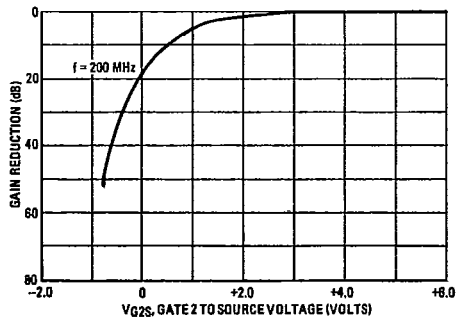


FIGURE 9 - CONVERSION POWER GAIN

